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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2186	3

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,475	ZITLAW, CLIFF	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The specification mentions "a synchronous bus 202", on page 4, in reference to figure 2. Number 202 does not appear in the figure.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 – 20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 21 of copending Application No. 09/943476 in view of Dye (US Patent No. 6,145,069).

4. With respect to claim 1, 6, 11, 16, 19, 20, the copending Application claims all of the limitations of the instant application except for the decompression circuit that decompresses the

data transferred from the non-volatile memory to the volatile memory. On the other hand, Dye discloses a processing system with a decompression circuit (figure 3, 280) that decompresses the data transferred from the non-volatile memory (100) to the volatile memory (160, 440).

It would have been obvious to one of ordinary skill in the art, having the teachings of Applicant's copending Application No. 09/943476 and Dye before him at the time the invention was made, to use the flash memory compression with a decompression engine teachings of Dye in the processing system of Application No. 09/943476, in order to provide improve data density, efficiency and bandwidth (Dye, col. 2, lines 42 – 46).

5. As to the dependent claims, while not all of them are identical, different combinations of dependent and independent claims with varying degrees of details in the copending application encompass subject matters claimed in the instant application.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the

invention. Claim 18 recites the limitation "the synchronous memory device" in line 1. There is insufficient antecedent basis for this limitation in the claim.

8. Claims 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims recite the limitations "the synchronous memory" and "the non-volatile memory". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, 3 – 5, 11, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Dye (US Patent No. 6,145,069).

With respect to claim 1, 3, 5, 11 and 14, Dye disclose a processing system comprising:

a processor (figure 3, 400);

a volatile memory device coupled to communicate with the processor (160, 420, 440);

a non-volatile memory device (900, 100) coupled to communicate with the processor and the volatile memory device, wherein the non-volatile memory device transfers data to the volatile memory device; and

a decompression circuit (280) provided in the non-volatile memory device to decompress the data while transferring to the volatile memory device.

11. With respect to claim 4 and 15, the processor is coupled to store compressed data in the volatile memory device (col. 12, lines 10 – 14).

12. Claims 11, 12, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Fallon *et al.* (US Patent Publication No. 2002/0069354, hereinafter "Fallon").

13. With respect to claim 11, Fallon discloses a processor system power-up method comprising:

initiating a data transfer from a non-volatile memory (figure 1, 11) to a volatile memory (13); and

decompressing (12) data stored in the non-volatile memory while transferring the data to the volatile memory (page 4, paragraph 42).

14. With respect to claims 12 and 18, the volatile memory device is an SDRAM (page 5, paragraph 49).

15. Claims 1, 4, 11 and 14 and are rejected under 35 U.S.C. 102(e) as being anticipated by Iverson (US Patent 6,332,172).

16. With respect to claim 1, Iverson discloses a processing system (figure 1) comprising:

a processor (1020);

a volatile memory device (104) coupled to communicate with the processor;

a non-volatile memory device (106) coupled to communicate with the processor and the volatile memory device, wherein the non-volatile memory device transfers data to the volatile memory device (figure 5); and

a decompression circuit provided in the non-volatile memory device to decompress the data while transferring to the volatile memory device (figure 6, 612).

17. With respect to claim 4, the processor is coupled to store compressed data in the volatile memory device (figure 4, see step 408, see also figure 9, step 908).

18. With respect to claims 11 and 14, Iverson discloses a processor system power-up method (figure 5) comprising:

initiating a data transfer from a non-volatile flash memory to a volatile memory ; and

decompressing data stored in the non-volatile memory while transferring the data to the volatile memory.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1, 2, 5 – 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari *et al.* (US Patent No. 6,266,724, hereinafter "Harari") in view of Fallon.

21. With respect to claims 1, 5, 6 and 9, Harari discloses a processing system (figure 1) comprising:

a processor (CPU in the host system 200) ;

a memory device coupled to communicate with the processor via a bus (figure 7, 41 and 60, or RAM in the host system);

a flash memory (20) device coupled to communicate with the processor via a serial bus col. 7,. Lines 34 – 36) and communicate with the memory device, wherein the flash memory device transfers data to the memory device (the flash daughter card is used as a non-volatile mass storage peripheral in Harari's disclosure, while not explicitly disclosed, the host system or a PC accesses data in the flash memory through a volatile memory, RAM, see col. 1 lines 23 – 35); and

a decompression circuit (Figure 5B, 42, col. 8, lines 56 – lines 62, see also col. 8, line 63 – col. 9, lines7) provided in the flash memory device to decompress the data while transferring to the memory device.

However, Harari does not specifically disclose that the memory device is synchronouns. On the other hand, Fallon discloses that modern computers use various forms of high speed memory such as a synchronous DRAM (page 1, paragraph 5).

It would have been obvious to one of ordinary skill in the art, having the teachings of Fallon and Harari before him at the time the invention was made, to use various forms of high speed memory including an SDRAM in a computer system with non-volatile memory as taught by Fallon in the computer system with non-volatile memory of Harari, in order to be able to choose from a wider variety of memories. One skilled in the art would easily recognize the benefit of being able to tailor the system depending on the need. For example, a synchronous DRAM is faster that a regular DRAM but costs more. For an applicant that requires higher speed, one would choose an SDRAM. For an application where the speed is not critical, a regular DRAM would be more cost effective.

22. With respect to claims 2 and 7, the memory device (Harari, figure 7, 41 and 60) initiates the data transfer (the controller 41 initiates the data transfer, note the direction of control).

23. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz *et al.* (US Patent No. 6,058,474, hereinafter "Baltz") in view of Harari.

Baltz discloses a processing system (figure 8) comprising:

a processor (10);

a synchronous memory device (23 and 100, col. 6, lines 7 – 9) coupled to communicate with the processor via a synchronous bus;

an EPROM memory device coupled to communicate with the processor via a bus and communicate with the synchronous memory device, wherein the EPROM memory device transfers data to the synchronous memory device (col. 7, lines 46 – 60); and

However, Baltz does not specifically disclose a flash memory that communicates via a serial bus and the decompression circuit. On the other hand, Harari discloses a processing system comprising a flash memory with the processor via a serial bus and a decompression circuit provided in the flash memory device to decompress the data while transferring to the synchronous memory device (see rejection of claim 6 above).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Harari before him at the time the invention was made, to use the flash memory and decompression teachings of the computer system that loads data from a flash EPROM of Harari in the computer system that loads data from an EPROM of Baltz, in order to provide a removable PC card that can accommodate components offloaded from the host system to minimize the size and cost of the host system and to provide flexibility in system configuration (Harari, col. 3, 31 – 35).

24. Claims 16, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Iverson.

Baltz discloses a processor system power-up method comprising:

detecting a power-up condition with a reset controller and providing a reset signal (figure 4A, 76, see also figure 8, RESET, DC11 – DC13) to an SDRAM memory (col. 6, lines 7 – 9, figure 8, 23 and 100);

using the SDRAM, initiating a data transfer from a non-volatile memory to the SDRAM memory in response to the reset signal; and providing a system reset signal from the synchronous memory to a processor after the data has been transferred (col. 7, lines 46 – 60).

However, Baltz does not specifically disclose a flash memory and that the method comprises decompressing of data stored in the non-volatile memory while transferring the data to the synchronous memory. On the other hand, Iverson discloses a method of loading a boot image from a flash memory that decompresses data stored in the non-volatile memory while transferring the data to a memory.

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Iverson before him at the time the invention was made, to use the boot load teachings of the computer system that boots from a non-volatile memory of Iverson in the computer system that boots from a non-volatile memory of Baltz, in order to reduce the system cost (Iverson, col. 2, lines 26 – 31). A compressed RAM image takes up less storage space.

25. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fallon in view of Shin (US Patent No. 6,735,669).

Fallon discloses all of the limitations of the parent claim 11 as discussed above. However, Fallon does not specifically disclose the use of RDRAM. On the other hand Shin discloses that RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Harari, Fallon, and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Harari and Fallon, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harari in view of Fallon as applied to claim 6 above further in view of Shin.

Harari and Fallon disclose all of the limitations of the parent claim as discussed above. However, they do not specifically disclose the use RDRAM. On the other hand Shin discloses that RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Harari, Fallon, and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Harari and Fallon, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

27. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Iverson as applied to claim 19 above further in view of Shin.

The only difference between claim 19 and claim 20 is the type of memory used. Balz and Iverson disclose all of the limitations of claim 19 as discussed above. However, they do not specifically disclose the use of RDRAM. On the other hand Shin discloses that RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Harari, Fallon, and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Harari and Fallon, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Culbert (US Patent No. 5,557,777) discloses a system that restores DRAM from a flash memory that stores compress data. Frank *et al.*(US Patent No. 6,546,489) disclose a computer system that transfers data from a non-volatile memory to a volatile memory and sends a control signal to the processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
May 5, 2004

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